



SHEET 1 OF 1

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
JP	6,026,286	15 Feb 00	Long	455	327	8/1/96

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JP	Mohan et al., "Modeling and characterization of on-chip transformers", Center for Integrated Systems, Stanford University, pp. 19.3.1-19.3.3 (undated)
JP	Zolfaghari, et al. "Stacked inductors and transformers in CMOS technology", (IEEE J. of Solid-State Circuits, vol. 36, No. 4, April 2001, pp. 620-628)
JP	Simburger, et al. "TP 13.6: a monolithic 3.7W silicon power amplifier with 59% PAE at 0.9 GHz (Feb. 1999, 4 pp)

EXAMINER

DATE CONSIDERED

01/22/03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.